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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,253	09/26/2001	Jeffrey Johnson	42390P12455	3010

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EXAMINER	
NGUYEN, DANNY	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/965,253	JOHNSON, JEFFREY	
	Examiner	Art Unit	
	Danny Nguyen	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 6/30/2005 have been fully considered but they are not persuasive.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Yue only lacks of having an ESD clamp circuit coupled to the inductor via the ESD circuit between supply and ground terminals. Waggoner discloses an ESD protection circuit comprises an ESD clamp circuit (B) coupled to the inductor (L) via the ESD circuit between supply and

ground terminals (112 and 114) to protect ESD phenomena. One of ordinary skill in the art at the time the invention was made would have recognized Waggoner's teaching and would have provided motivation to an ESD designer as well.

Applicant also argued that Waggoner does not disclose an ESD clamp circuit coupled to the inductor via the ESD circuit. The argument is not persuasive. Waggoner clearly teaches that an ESD clamping circuit (B) is coupled to an inductor (L) via an ESD circuit (diode Ds) (see figure 7).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 5-7, 9-12, 15-17, 19-22, 25-27, 29, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yue et al. (USPN 6,509,779) in view of Waggoner et al (USPN 6,034,400).

Regarding claims 1, 4, 10, 11, 14, 20, 24, Yue discloses a method and an apparatus (see figures 3 and 4) comprises an inductor (110) having an impedance connected in series between an output of a high frequency circuit (20) operating at a frequency and an ESD circuit (40) configured to protect the high frequency circuit from an ESD event, the impedance having substantially high value at that frequency and a substantially low value at the ESD event (e.g. col. 3 and 4, lines 63-4). Yue does not

disclose an ESD clamping circuit as claimed. Waggoner discloses an ESD protection circuit (e.g. see fig. 7) comprises an ESD clamp circuit (B) is connected to an inductor (L) via an ESD circuit (such as diode Ds) between supply and ground terminals (112 and 114) to protect electrostatic discharge phenomena (e.g. col. 7, lines 27-61 and col. 11, lines 1-4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified to the ESD protection circuit of Yue to incorporate the ESD clamping circuit as taught by Waggoner in order to protect the IC circuit against over- voltage appearing at supply terminal (col. 5, lines 13-17).

Regarding claims 21, 30, Yue discloses a circuit (such as fig. 3 and 4) comprises a high frequency circuit operating at a frequency (e.g. 100), the high frequency circuit having an output (20); an electrostatic discharge ESD circuit (40) configured to protect the high frequency circuit from an ESD event (col. 4, lines 9-15); an inductor (110) having an impedance connected in series between an output of a high frequency circuit (20) operating at a frequency and an ESD circuit (40) configured to protect the high frequency circuit from an ESD event, the impedance having substantially high value at that frequency and a substantially low value at the ESD event (e.g. col. 3 and 4, lines 63-4). Yue does not disclose an ESD clamping circuit as claimed. Waggoner discloses an ESD protection circuit (e.g. see fig. 7) comprises an ESD clamp circuit (B) is connected to an inductor (L) via an ESD circuit (such as diode Ds) between supply and ground terminals (112 and 114) to protect electrostatic discharge phenomena (e.g. col. 7, lines 27-61 and col. 11, lines 1-4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified to the ESD protection

circuit of Yue to incorporate the ESD clamping circuit as taught by Waggoner in order to protect IC circuit against over- voltage appearing at supply terminal (col. 5, lines 13-17).

Regarding claims 2, 12, 22, Yue discloses the ESD circuit (40) has first and second terminals, the first terminal being connected to one end on the inductor (110), and the second terminal being connected to ground (shown in fig. 3).

Regarding claims 5, 15, 25, Yue et al. disclose the inductor is connected between a first bond pad (10) of the output and a second bond pad (10a) of the ESD circuit (40) on a package substrate in a package encapsulating the high frequency circuit (100d) and the ESD circuit (40) (see fig. 13).

Regarding claims 6, 16, 26, Yue discloses connecting the inductor (110) comprise connecting one end of the inductor to the first bond pad (10) via a first bond wire; and connecting an other end of the inductor to the second bond pad (10a) via a second bond wire.

Regarding claims 9, 19, 29, Yue discloses the high frequency higher than 1 gigahertz (col. 4, lines 24-25).

Regarding claim 7, 17, 27, Yue et al. disclose the high frequency circuit and ESD circuit are on a silicon die mounted on the package substrate (see abstract).

3. Claims 3, 13, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yue in view of Waggoner, and Kleveland et al (USPN 5,969,929). Yue and Waggoner do not disclose the ESD circuit is a gate grounded NMOS and a diode. Kleveland discloses an ESD circuit being a gate grounded NMOS (such as 330 shown in fig. 3B).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the ESD circuit of Yue and Waggoner incorporate a GGNMOS as taught by Kleveland because the ESD circuit (330) of Kleveland provides less components and higher trigger voltage, so it can save space and provide a better ESD protection.

4. Claims 8, 18, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yue et al in view of Waggoner et al, and Chiu (USPN 6,414,849). Yue and Waggoner do not disclose the package is flip-chip BGA package. Chiu discloses the package is flip-chip BGA package (col. 5, line 35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the integrated circuit of Yue and Waggoner to use a flip-chip BGA package as taught by Chiu in order to reduce stress in the IC circuit (Chiu, col. 5, lines 48-51).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Danny Nguyen whose telephone number is (571)-272-2054. The examiner can normally be reached on Mon to Fri 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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9/7/2005

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER